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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/822,784	04/13/2004	Wei-Chi Lu	GEN0021-US	3197

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EXAMINER	
MISIURA, BRIAN THOMAS	
ART UNIT	**PAPER NUMBER**
2111	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/822,784	LU, WEI-CHI	
	Examiner	Art Unit	
	Brian T. Misiura	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Action

Response to Arguments

1. Applicant's arguments, see page 9, filed 1/10/2007, with respect to the rejection of claim(s) 1, 10, and 20, specifically limitation "and when both said first host and said second host are effectively interfaced with said apparatus, said storage medium is appended to one of said first host and said second host and said apparatus provides...access to said storage medium from both said first host and said second host." have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made.

2. Applicant's arguments, page 9, paragraph 2, with respect to the secondary reference, Perry et al. (2003/0236910), have been fully considered but are not persuasive. The applicant states:

> Moreover, Perry discloses that "[t]he host-to-host (HTH) message passing procedure...is mediated by the DCU 12" and "the DCU 12 need not read, interpret or otherwise act on the message payload" in paragraph 27. To the contrary, the buffer circuit of the present application needs to be "interfaced with said first hot plug/hot swap interface, said second hot plug/hot swap interface and said storage interface so as to process data among said first host, said second host and said storage medium," as recited in claims 1, 10, and 20. Nowhere in Perry is there disclosed the data processing procedure among the hosts and the storage medium."

3. The Examiner respectfully disagrees with this viewpoint. Referring to Claim 1, "a buffer circuit interfaced with said first hot plug/hot swap interface, said second hot plug/hot swap interface and said storage interface so as to process data among said first host, said second host and said storage medium", the Examiner points out that a buffer circuit, as described by the Applicant on page 7 of the Specification and as well know in the art, is that of a FIFO unit. A FIFO unit

is one that stores/removes data entries in the order in which they are entered into the buffer. Therefore, the only "processing data among said first host, said second host and sad storage medium" that could possibly take place is that of storing and removing items from the buffer. The Examiner cites paragraphs 27, 33, and 35 of Perry to disclose the buffer circuit partaking in receiving/removing entries from the buffer in the processes of interacting with the hosts and storage unit.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin, U.S. Patent Application No. 10/063,777 in view of Perry et al. U.S. Patent Application Publication No. 2003/0236910 in further view of Conner et al. U.S. Patent No. 5,867,686.

5. Per claims 1, 10, Lin discloses: an apparatus for multiple host access to a storage medium, comprising:

- a first hot plug/hot swap interface for interfacing to a first host (figure 2 numeral 32);
- a second hot plug/hot swap interface for interfacing to a second host (figure 2 numeral 36);
- a storage interface for interfacing to said storage medium (paragraph 20, figure 2 numeral 42a);
- a control circuit for controlling access to said storage medium from said first host and said second host (figure 2 numeral 42),
- so that, when only one of said first host and said second host is effectively interfaced with said apparatus, said storage medium is appended to said effectively interfaced host and said apparatus provides access to said storage medium from said effectively interfaced host (paragraph 22, figure 2),
- and when both said first host and said second host are effectively interfaced with said apparatus, said apparatus provides bridging between said first host and said second host (paragraphs 24 and 26, figure 2)

Lin does not disclose when both said first host and said second host are effectively interfaced with said apparatus, said storage medium is appended to one of said first host and said second host, and as well as access to said storage medium from both said first host and said second host.

- However, Conner discloses a mass storage device **102** shared among multiple hosts **104**, including one of the hosts being designated as a channel master, which has privileges over the other hosts (column 27 lines 13-23). Also, Connor discloses hosts with the ability to lock specific address space within the mass storage device. However, even though the address storage is locked

(appended to a host) the data within the space is always readable by another host (lines 19-30 – figures 1-3).

- It would have been obvious to one having ordinary skill in the art at the time of the applicants claimed invention to incorporate the address space locking of Connor into the system of Lin as additional operational mode which a host to access a storage device even when a second host is attached to that storage device. Lin evidences the combination of these two systems as welcome in paragraph 20 stating, "the present invention is not limited to the aforementioned two functions, however, and many combinations are possible."

Lin does not disclose a buffer circuit interfaced with said first hot plug/hot swap interface, said second hot plug/hot swap interface and said storage interface so as to process data among said first host, said second host, and said storage medium.

- However, Perry discloses a Message Buffer (paragraph 27, figure 1 numeral 20) interfaced with a first and second host (figure 1 numeral 16), and a mass storage unit (paragraph 20 figure 1 numeral 14), and acts in the process of data among the hosts' and the mass storage unit (paragraph 33 and 35, figure 1)

- It would have been obvious to one having ordinary skill in the art at the time of the applicant's claimed invention to incorporate the teaching of Perry into the system of Lin to have a single buffer circuit instead of numerous buffer circuits. The modification would have been obvious because one having ordinary skill in the art would want to reduce the number of buffer circuits in their system in order to save both space and cut down the cost of production.

6. Per claims 2 and 12, Lin does not disclose wherein when both said first host and said second host are effectively interfaced with the apparatus, said storage medium is appended to the first effectively interfaced one of said first host and said second host.

- However, Conner discloses that on a first come basis, address space of the mass storage device is locked to a requesting host (appended thereto) (lines 19-30 – figures 1-3).

- It would have been obvious to one having ordinary skill in the art at the time of the applicants claimed invention to incorporate the address space locking of Connor into the system of Lin as additional operational mode which a host to access a storage device even when a second host is attached to that storage device. Lin evidences the combination of these two systems as welcome in paragraph 20 stating, "the present invention is not limited to the aforementioned two functions, however, and many combinations are possible."

7. Per claims 3 and 13, Lin discloses wherein said control circuit comprises a detecting circuit for detecting interface states of said first host and said second host (paragraph 20, figure 2 numeral 40) and a switching circuit for switching the appending of said storage medium to said first host or to said second host (paragraph 20, figure 2 numeral 42 "control circuit").

8. Per claims 4, 14, and 21, Lin discloses: the apparatus for multiple host access to a storage medium of claim 1, wherein said first hot plug/hot swap interface and said second hot plug/hot swap interface are USB (Universal Serial Bus) interfaces (paragraph 20 figure 2).

9. Per claims 5, 15, and 22, Lin does not disclose the hot plug/hot swap interfaces are IEEE 1394 interfaces.

- However, it would have been obvious to one having ordinary skill in the art at the time of the applicant's claimed invention to use a Firewire interface rather than USB since both methods are very similar and both can be the ideal choice in different systems.

10. Per claims 6, 8, 16, and 18, Lin does not disclose wherein the medium is a mass storage device/hard disk drive.

- However, Perry discloses: wherein said storage medium is a mass storage device/hard disk drive (paragraph 20).

- It would have been obvious to one having ordinary skill in the art at the time of the applicant's claimed invention to incorporate the teaching of Perry into the system of Lin to provide a means of non-volatile storage for the hosts to access.

11. Per claims 7 and 17, Lin discloses: the apparatus for multiple host access to a storage medium of claim 1, wherein said storage medium is a memory device (paragraph 20, particularly "operational mode A **42**a is a permanent storage device (such as a flash memory stick)").

12. Per claims 9 and 19, Perry discloses a buffer circuit as described in claim 1, however Perry does not disclose that the buffer circuit is a FIFO buffer.

Lin discloses two separate buffers, each being FIFO buffers (paragraph 20, figure 2 numeral 34 and 38).

- It would have been obvious to one having ordinary skill in the art at the time of the applicant's claimed invention to incorporate the teaching of Perry into the system of Lin to have a FIFO buffer handle the transactions of the system.
- The modification would have been obvious because one having ordinary skill in the art would want to use a buffer that demonstrates a method of priority in which data/messages are processed, which a FIFO buffer demonstrates as disclosed in Lin.

13. Per claim 11, Lin does not disclose a plurality of storage interfaces and storage media.

- However, Perry discloses wherein, said apparatus comprises a plurality of storage interfaces for interfacing to a plurality of storage media (paragraph 20 – plurality of disk drives arranged in ranks or arrays).

- It would have been obvious to one having ordinary skill in the art at the time of the applicant's claimed invention to incorporate the teaching of Perry into the system of Lin to provide multiple storage means allowing for more total storage capacity.

14. Claims 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin, U.S. Patent Application No. 10/063,777, in view of Perry et al. U.S. Patent Application Publication No. 2003/0236910 in further view of Connor et al. U.S. Patent No. 5,867,686, in further view of Luke et al. U.S. Patent No. 6,233,640.

15. Per claim 20, Lin discloses: an apparatus for multiple host access to a storage medium, comprising:

- a first hot plug/hot swap interface for interfacing to a first host (figure 2 numeral 32);
- a second hot plug/hot swap interface for interfacing to a second host (figure 2 numeral 36);
- a storage interface for interfacing to said storage medium (paragraph 20, figure 2 numeral 42a);
- and a control circuit for controlling access to said storage medium from said first host and said second host (figure 2 numeral 42),
- so that, when only one of said first host and said second host is effectively interfaced with said apparatus, said storage medium is appended to said effectively interfaced host and said apparatus provides access to said storage medium from said effectively interfaced host (paragraph 22, figure 2),
- and when both said first host and said second host are effectively interfaced with said apparatus said apparatus provides bridging between said first host and said second host (paragraph 20, particularly "whereas operational mode B **42**b is a host-to-host linking device.", paragraph 26, figure 2 numeral 42b).

Neither Lin nor Perry disclose: when both said first host and said second host are effectively interfaced with said apparatus, said storage medium is appended to one of said first host and said second host; said apparatus provides access to said storage medium from both said first host and said second host

- However, Conner discloses a mass storage device **102** shared among multiple hosts **104**, including one of the hosts being designated as a channel master, which has privileges over the other hosts (column 27 lines 13-23). Also, Connor discloses hosts with the ability to lock specific address space within the mass storage device. However, even though the address storage is locked (appended to a host) the data within the space is always readable by another host (lines 19-30 – figures 1-3).

- It would have been obvious to one having ordinary skill in the art at the time of the applicants claimed invention to incorporate the address space locking of Connor into the system of Lin as additional operational mode which a host to access a storage device even when a second host is attached to that storage device. Lin evidences the combination of these two systems as welcome in paragraph 20 stating, "the present invention is not limited to the aforementioned two functions, however, and many combinations are possible."

Lin does not disclose a buffer circuit interfaced with said first hot plug/hot swap interface, said second hot plug/hot swap interface and said storage interface so as to process data among said first host, said second host, and said storage medium.

- However, Perry discloses a Message Buffer (paragraph 27, figure 1 numeral 20) interfaced with a first and second host (figure 1 numeral 16), and a mass storage unit (paragraph 20 figure 1 numeral 14), and acts in the process of data among the hosts' and the mass storage unit (paragraph 33 and 35, figure 1)

- It would have been obvious to one having ordinary skill in the art at the time of the applicant's claimed invention to incorporate the teaching of Perry into the system of Lin to have a single buffer circuit instead of numerous buffer circuits. The modification would have been obvious because one having ordinary skill in the art would want to reduce the number of buffer circuits in their system in order to save both space and cut down the cost of production.

Neither Lin nor Perry disclose: a cable having at one end a third connector for connecting to said second connector and at the other end a forth connector for connecting to said second host.

- However, Luke discloses: a cable having at one end a third connector for connecting to said second connector and at the other end a fourth connector for connecting to said second host (Luke, figure 1 numeral 14)

- It would have been obvious to one having ordinary skill in the art at the time of the applicant's claimed invention to incorporate the teaching of Luke into the system of Lin and Perry to provide a cable for allowing a greater distance between the host devices.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian T. Misiura whose telephone number is (571) 272-0889. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (571) 272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brian Misiura
2/15/2007

Paul R. Myers
PAUL R. MYERS
PRIMARY EXAMINER